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INVESTIGATION OF LOW TEMPERATURE MULTILEVEL DIELECTRICS FOR APPLICATION FOR RADIATION TOLERANT, SUBMICRON-SCALED IC TECHNOLOGY

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The following report details the progress on ONR contract number N-00014-86-C-0421 during the period from January 1, 1991 to December 31, 1991. This program entails a joint effort between Research Triangle Institute and North Carolina State University. Funding is being provided by the Innovative Science and Technology Office of the Strategic Defense Initiative. The objective of this program is to develop deposited, multilayer dielectric structures for integrated circuit applications requiring reliable radiation tolerant insulators.

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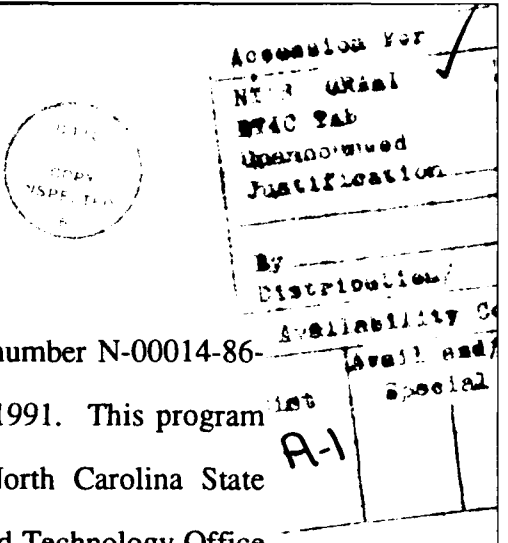


1.0 INTRODUCTION

The following report details the progress on ONR contract number N-00014-86-C-0421 during the period from January 1, 1991 to December 31, 1991. This program entails a joint effort between Research Triangle Institute and North Carolina State University. Funding is being provided by the Innovative Science and Technology Office of the Strategic Defense Initiative. The objective of this program is to develop deposited, multilayer dielectric structures for integrated circuit applications requiring reliable radiation tolerant insulators.

The primary goal of this program is to develop low temperature processes for use in the formation of highly reliable, radiation tolerant MOS structures utilizing deposited insulator structures. The tasks include development of in situ surface cleaning techniques and low temperature insulator deposition techniques. The low temperature processing technology is based on remote plasma enhanced activation of reactions. Progress during this year has been made in 3 different areas, 1) analysis of the Si/SiO_2 interface formation process at low temperature (300 °C), 2) the effect of plasma power on oxide and nitride film properties, 3) testing of the radiation tolerance of the oxides, nitrides, and oxide-nitride-oxide films.

The formation process of the Si/SiO_2 interface is critical to the electrical quality and integrity of the interface. Experiments have been performed using Xray Photoemission Spectroscopy to analyze the process during the first few monolayers of oxide deposition. It was found that about 5 angstroms of Si was consumed by plasma oxidation prior to formation of deposited oxide. This result indicates that the formation of a high quality electrical interface depends on proper low temperature oxidation of the Si surface. Further experiments have shown that intentional plasma oxidation of the silicon surface can result in the formation of an Si/SiO_2 interface which exhibits low interface state density ($1\text{-}2 \times 10^{10}\ cm^{-2}eV^{-1}$) and good minority carrier lifetime. Studies

investigating the effect of plasma power on the film properties have shown that films with structural properties closer to those of high temperature films can be deposited using high plasma power density. The high power density allows deposition of films at higher rates while still maintaining good bulk characteristics. Higher deposition rates allow higher through put of wafers in single wafer processing operations. Statistical analysis of breakdown voltage vs. capacitor area indicate that the dominant breakdown mechanism is particulate related and not an intrinsic property of the dielectric film.

The radiation hardness of the oxide, nitride and oxide-nitride-oxide films have been investigated. It was found that the composite films showed promising radiation tolerance. With a 1 Mrad Xray dose, the flatband voltage shifted by only 30 to 70 mV while D_{it} increased by only 1×10^{10} $cm^{-2}eV^{-1}$. This is a state of the art result for a low temperature dielectric film and is reasonably close to the performance of thermal SiO_2. For applications requiring very low processing temperature and radiation hard behavior, such as deep sub-micron MOSFETs or devices containing Si-Ge elements, this dielectric material may provide a needed alternative to thermal oxidation.

The anticipated payoffs for this work are twofold. First, the anticipated result is a new viable processing technology for low temperature gate insulator formation. The deposition technology provides flexibility for formation of multilayer insulator structures with controlled compositions not available with conventional thermal oxidation processes. Second, the structural and complementary electrical characterization of the films have in fact led to new insights as to the physical origins of defect structures in the films. Such insights may be helpful in further improving the reliability of dielectric insulators across the board.

2.0 REACTOR SCALING

During the previous year scaling studies were carried out using the 5.8 inch diameter reactor at RTI. This reactor design was capable of accepting 3, 4 and 5 inch wafers. It was found that uniformity over a 3 inch wafer was on the order of 5%, with the 4 and 5 inch wafers showing increasingly worse uniformity. The flats on the 5 inch wafer were clearly causing conductance changes in the flow path through the reactor. These results indicated that the uniformity of deposition in the reactor was limited to a large extent by gas flow restriction causing flow nonuniformity. The 3 inch wafer results indicated that the reactor tube diameter should be about twice the diameter of the wafer. A new design for the reactor tube with a large diameter region in the vicinity of the wafer has been implemented. This new design is aimed partly at reengineering the heating configuration to increase heating efficiency, thereby allowing investigation of higher temperature processes.

This new reactor configuration will allow mix and match processes consisting of plasma active processes and rapid thermal processes to be performed. Processes will include: plasma activated in situ cleaning and dielectric deposition, in conjunction with rapid thermal oxidation and annealing. In addition, hybrid processing utilizing plasma derived species to drive high temperature processes will be investigated.

3.0 EFFECT OF PLASMA POWER ON DEPOSITED FILMS

It has been found that the properties of oxide and nitride film deposited by remote plasma enhanced deposition depend on the rate of the deposition process and the process conditions under which a film is formed. It has been found that the plasma power can have a strong effect on the physical properties of the deposited films. The effect of plasma power on oxide deposition has been investigated. This study was to investigate the properties of films deposited at various power levels as a function of deposition rate.

Plasma power levels ranging from 10 to 300 watts were investigated. As shown in Figure 1 the deposition rate of oxide at a given silane flow was found to be a strong function of plasma power at low power levels. At higher power levels and lower silane flow the deposition rate leveled off then slightly decreased. At higher silane flow the rate continued to increase with power. As shown in Figure 2, the etch rate of the deposited oxide was found to be a strong function of deposition power and silane flow. Etch rates approaching those of thermal oxide were obtained at the 300 watt power level. Higher power is needed to maintain constant etch rate for films deposited at a higher silane flow (higher deposition rate). Likewise the index of refraction was found to be a strong function of plasma power and silane flow (deposition rate) as shown in Figure 3. Refractive indexes approaching those of thermal oxide were obtained at higher plasma powers. Again, at higher deposition rates, higher power was needed to maintain the same index.

The electrical properties of films deposited at various power levels and deposition rates were investigated. No clear trend was observed. Films with similar electrical properties were formed under all conditions. Short loop process insertion experiments were carried out with the Microelectronics Center of North Carolina (all fabrication and testing costs were born by MCNC). The insertion experiment was design to produce poly silicon gated devices using the deposited oxides and ONO structures. Process

insertion experiments clearly showed that the robust etching properties of the high power films are necessary to use the films in a poly gate process. Low power films inserted into the poly gate process resulted in shorted capacitors. High power films used in the process yielded some working capacitors. The same power dependence was found for ONO structures. Further investigation is required to produce films suitable for insertion in a standard poly gate process.

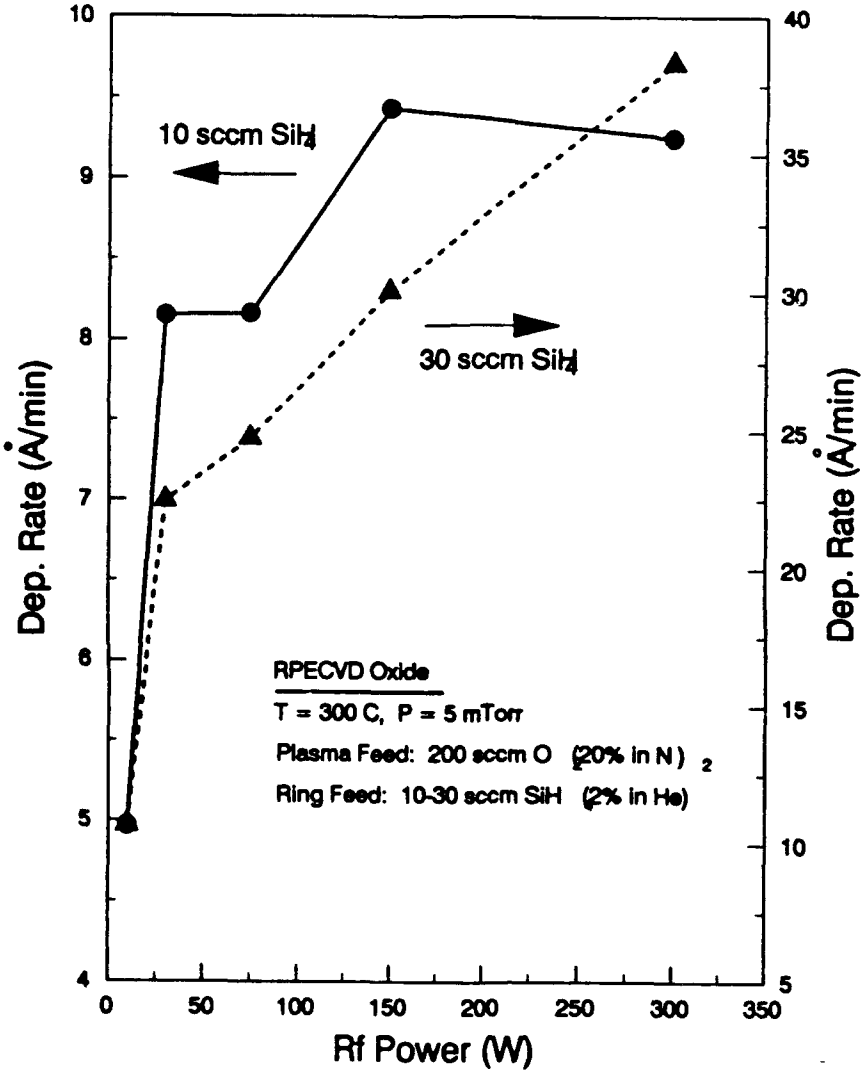


Figure 1 **Oxide deposition rate vs. Rf power**

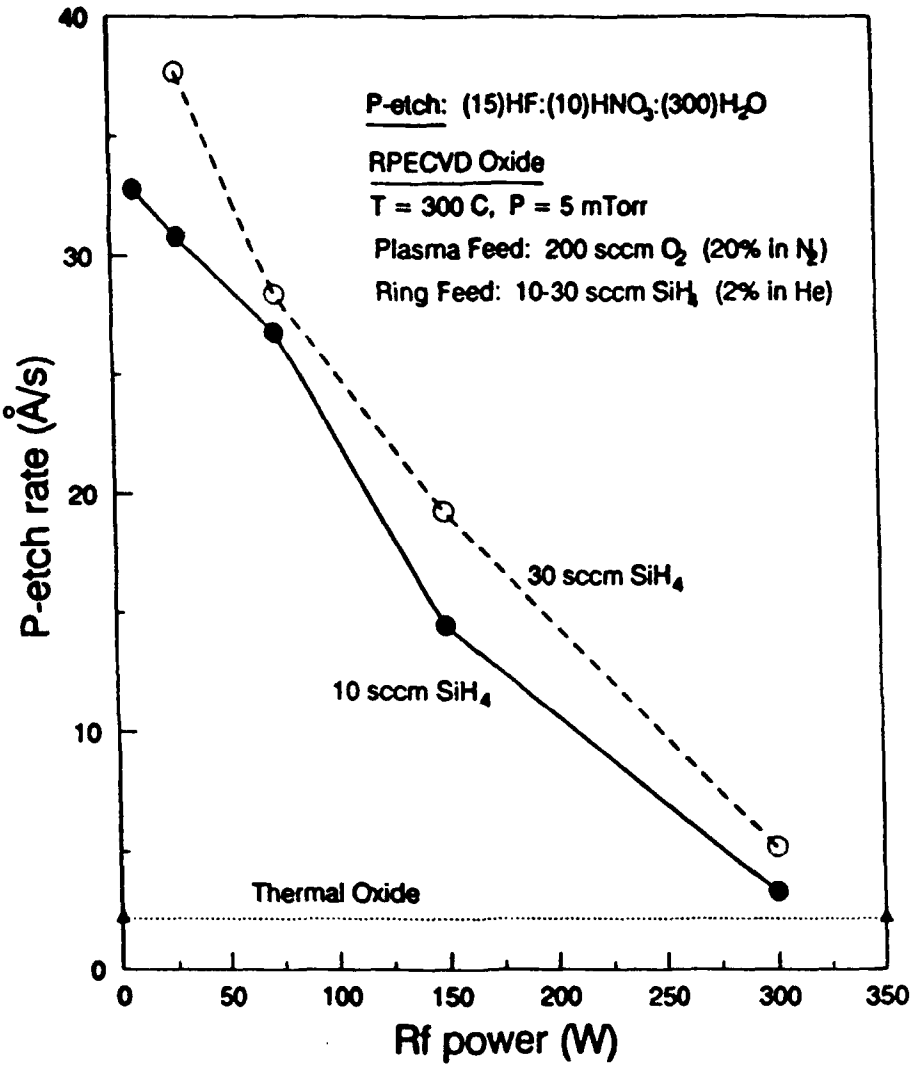


Figure 2 **P-etch rate vs. Rf Power**

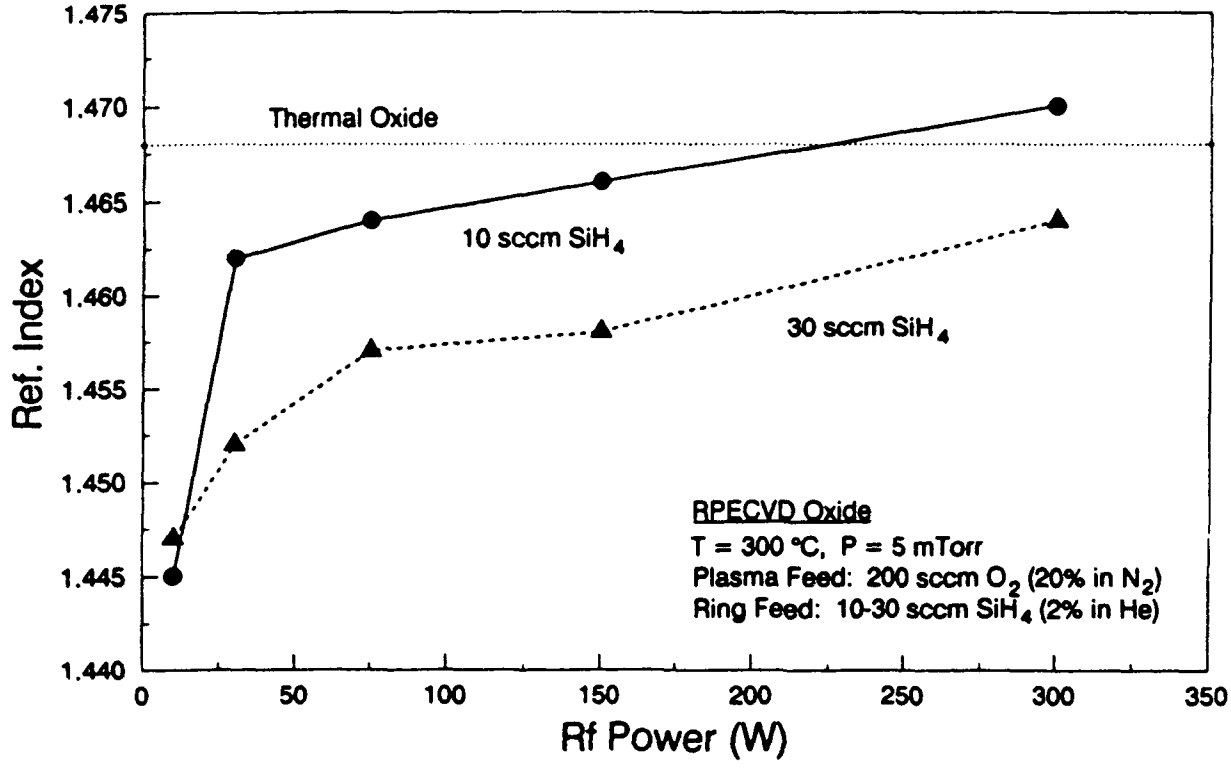


Figure 3 **Ref. Index versus Rf Power**

4.0 IN SITU HYDROGEN CLEANING PROCESS

Development of the hydrogen cleaning process has continued. If performed properly, this process can produce a clean Si surface free of oxygen and carbon, with no surface roughening. Long hydrogen treatments at temperatures below 450 °C will result in unacceptable surface etching. The hydrogen cleaning process is not very effective at removing SiO_2. Thus a properly prepared, hydrogen terminated Si surface, as can be attained with a dilute HF dip, is necessary for maximum in situ cleaning effectiveness. While simultaneous oxidation and carbon removal has been shown acceptable for oxide film formation, a cleaning process which leaves the Si surface clean and free of oxide is essential for epitaxial deposition processes.

Studies have shown that leaving a Si surface hydrogen terminated while the sample is being handled or stored in the vacuum integrated environment, can help keep the surface free of carbon and oxygen contaminants. Samples were cleaned in situ to remove carbon and oxygen to levels below the detectability limits of Auger and XPS analysis techniques, and then stored in the RTI integrated processing and analysis system. One sample was annealed to remove the hydrogen from the surface. Despite the fact that the samples were sitting in a 10^{-9} torr vacuum level, some oxygen contamination was observed. The hydrogen terminated sample, stored for 72 hours, had 3 times less oxygen than the sample with no hydrogen termination which was stored for 48 hours.

5.0 DIRECT PLASMA OXIDATION STUDIES

During this past year oxidation of the Si surface by oxygen plasma has been investigated from two aspects. First, the initiation of the plasma deposition process was studied using XPS analysis of special samples with 2.5 nm of Si deposited on a Ge substrate. By analyzing the attenuation of the Ge and Si XPS signals, consumption of the Si layer by oxidation could be monitored. It was found that approximately 0.5 nm of the Si layer was consumed during the initiation of the deposition process and that oxide deposition was suppressed during this oxidation phase. The initial phase resulted in formation of 1.5 nm of oxide, 1.1 nm from oxidation and 0.4 nm from deposition. During a second deposition cycle, 1.6 nm of oxide was deposited and no Si was consumed. Thus it was concluded that it is virtually impossible to deposit SiO_2 using the remote plasma process (and likely any other plasma activated process) without oxidizing the substrate to some extent during the initial phases of the deposition process. Thus the second aspect of the investigation, which followed from the first aspect, was related to optimization of the interfacial oxidized layer. This was accomplished by directly oxidizing the surface with an oxygen plasma. The investigation performed involved use of the in situ cleaning process followed by direct plasma oxidation. The samples formed in this way showed superior lifetime compared to those formed without the direct oxidation step. In addition, the process used resulted in relatively low interface state densities at process temperatures as high as 400 °C as shown in Figure 4. (Higher temperatures have not been investigated.)

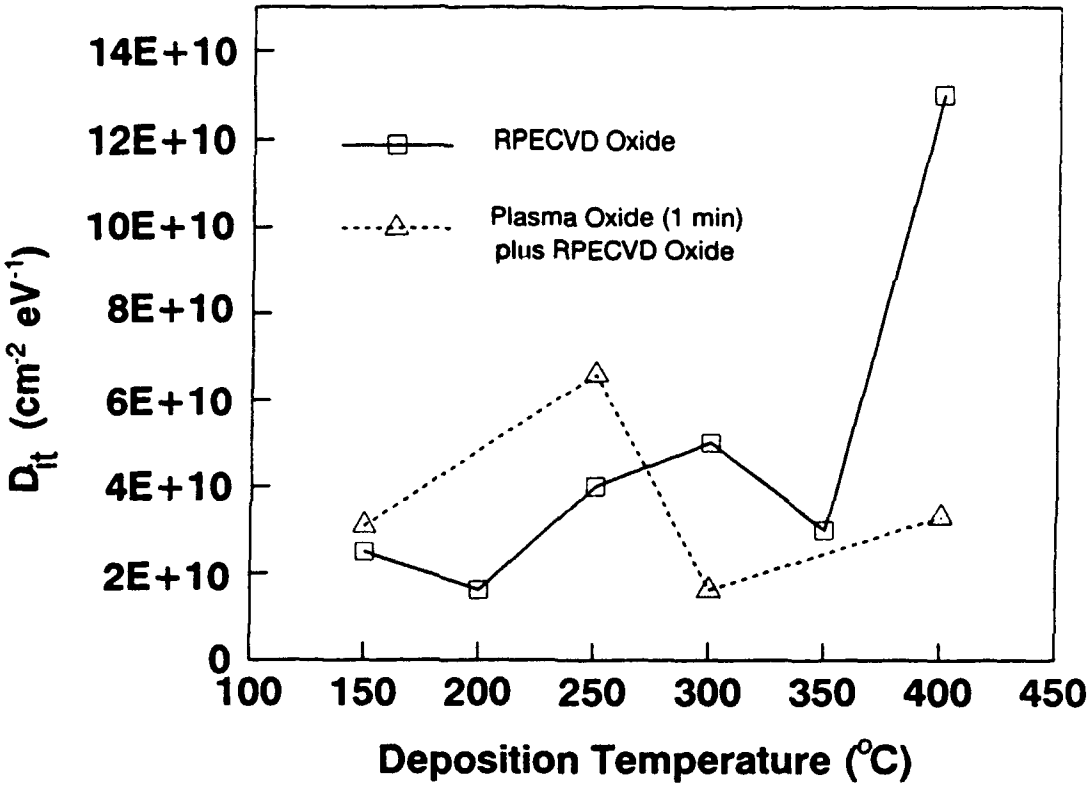


Figure 4 **D_{it} versus Deposition Temperature**

6.0 ONO STACKED STRUCTURE FORMATION

A recipe is being developed for the formation of reliable deposited ONO dielectric structures. This recipe is outlined as follows:

Interface Formation and Oxide Deposition

- **In situ Cleaning**
  - **Surface contaminants must be removed without damaging the Si surface**
- **Surface oxidation**
  - **Si surface oxidation is unavoidable with the deposition process**
  - **Controlled Si surface oxidation improves interfacial character**
  - **Thermal oxidation (future area of investigation)**
  - **Direct plasma assisted oxidation (current area of investigation)**
- **Oxide layer deposition**
  - **Important deposition parameters: plasma power, temperature, deposition rate**
  - **Nitrogen is incorporated in the interfacial oxide layer during nitride deposition.**
  - **Controlled nitrogen incorporation may be important for robust electrical properties however nitrogen increases D_{it}**
  - **Post deposition processing may be necessary to optimize performance and reliability (nitridation, annealing)**

Nitride Deposition

- Down stream nitride deposition process
  - Down stream N_2-SiH_4 based process
  - Remotely generated Ar plasma drives reaction
- Important deposition parameters:
  - Plasma power (higher power leads to higher film density and lower H content)
  - Temperature (higher temperature leads to lower H content and higher density)
  - Deposition rate (lower deposition rate leads to higher density and lower H content)
  - The use of higher power and higher temperature allows higher deposition rate
- Deposition environment must be oxygen free to obtain robust electrical properties
  - Typical ON structure formation requires a pump/purge cycle between oxide and nitride
  - Proper gas feed design and chamber design can reduce pump purge cycle time
- Necessary nitride physical properties
  - High density
  - Low etch rate
  - Good diffusion barrier
- Necessary electrical properties
  - High charge to breakdown
  - Low charge trapping and low fixed charge

A new concept which has recently come to bear on the recipe is listed under the oxide layer deposition items, i.e. the incorporation of nitrogen in the interfacial oxide layer. Indirect evidence of nitrogen intermixing is derived from the higher interface state densities often noted with ONO structure with thin interfacial oxides. Direct evidence of this intermixing was derived from parallel electron energy loss spectroscopy performed courtesy of Arizona State University. Data from this experiment indicates that nitrogen is found throughout a 1 nm interfacial oxide layer. Coupled with the finding of enhanced radiation resistance of the ONO samples, this finding suggests that proper nitrification of the interfacial oxide layer is essential for reliability as illustrated in Figure 5. Future deposition experiments will be carried out to further investigate this possibility.

Characteristics of ONO stacked structures deposited using various conditions are shown in Figures 6 through 8. The best result in terms of charge to breakdown seen from these various conditions was obtained using low deposition rates to form the structures. Structures formed using higher deposition rates and using plasma oxidation exhibited charge to breakdown values over an order of magnitude below those of the structure deposited at low rates.

Breakdown hystograms comparing the statistical breakdown performance of a deposited oxide, a thermal oxide and a deposited ONO structure are shown in Figures 9 through 11. It is clear that the ONO structure out performs the deposited oxide and the thermal oxide. This performance may be indicative of the resistance of the ONO structure to degradation by the Aluminum gate electrode.

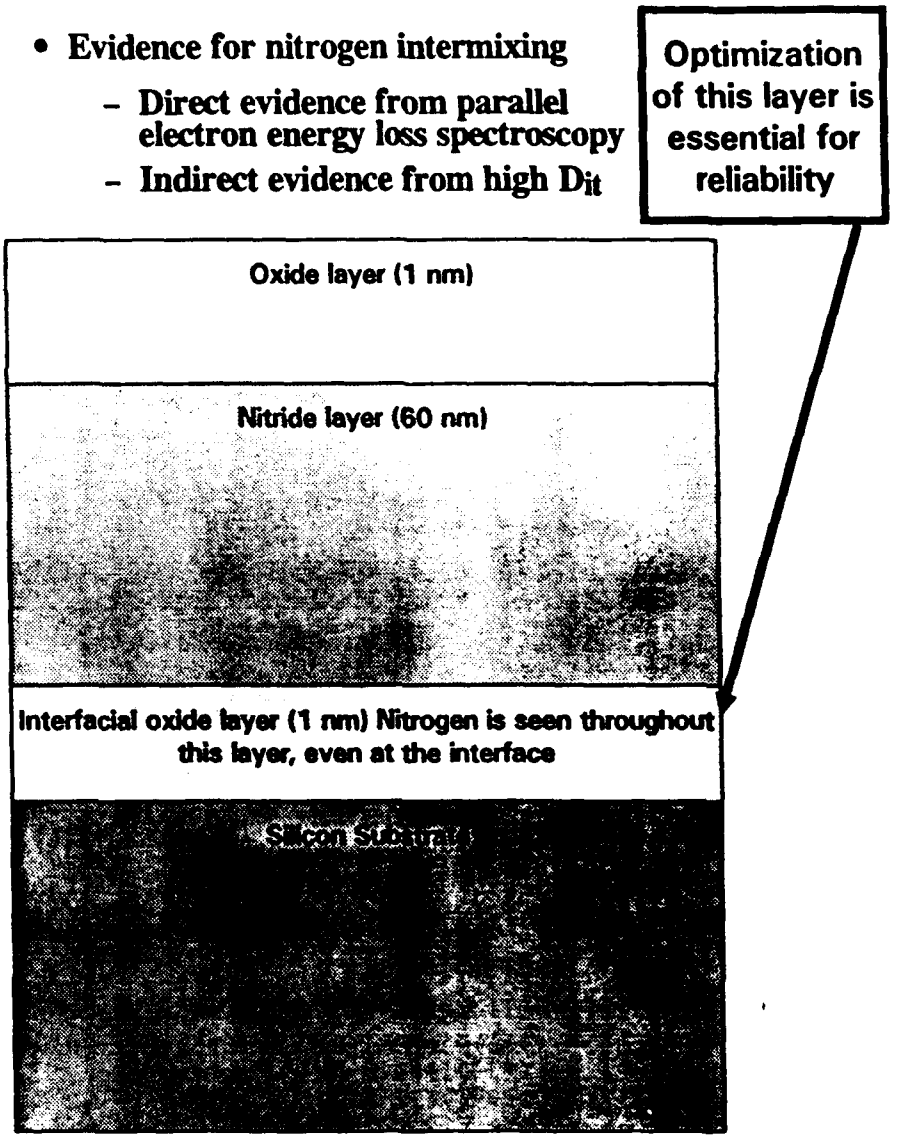


Figure 5

Nitrogen Intermixing in the Interfacial Oxide Layer

- Formation conditions
  - Plasma Power: 30(oxide), 30(nitride) watts
  - Temperature: 300°C
  - Pump/purge cycle time: 15 min with 500 sccm Ar flow at about 0.1 torr
  - Oxide Deposition rate: 4 Ang/min
  - Nitride deposition rate: 0.9 Ang/min
- Properties
  - Equivalent oxide thickness: 71 Ang
  - Midgap Dit: 0.9 to $1x10^{11}cm^{-2}eV^{-1}$
  - Hysteresis: 100 mV
  - Ave Breakdown field: 11 MV/cm
  - Flatband Voltage: -0.5 V

Charge to Breakdown Summary

- Test Capacitor Area $5x10^{-5}$ cm^2
- Current Density: 0.36 A/cm^2
- Oxide Eq Stress Field: 11 MV/cm
- Polarity: Negative gate bias
- Total Charge : 179 C/cm^2

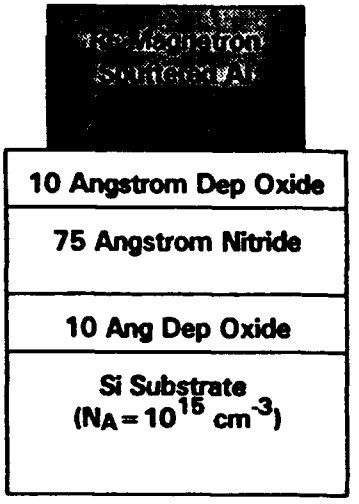


Figure 6 **RPECVD ONO Stack - Low Deposition Rates**

- Formation conditions
  - Plasma Power: 200(oxide), 200(nitride) watts
  - Temperature: 300°C
  - Pump/purge cycle time: 5 min high vacuum
  - Oxide Deposition rate: 24 Ang/min
  - Nitride deposition rate: 8 Ang/min
- Properties
  - Equivalent oxide thickness:
  - Midgap Dit: 3 to $4x10^{11} cm^{-2} eV^{-1}$
  - Hysteresis: 15 mV
  - Ave Breakdown field: 13.8 MV/cm
  - Flatband Voltage: -1.20 V

Charge to Breakdown Summary

- Test Capacitor Area $5x10^{-5}$ cm^2
- Current Density: $1.6x10^{-2}$ A/cm^2
- Oxide Eq Stress Field: 13.8 MV/cm
- Polarity: Negative gate bias
- Total Charge : 6.6 C/cm^2

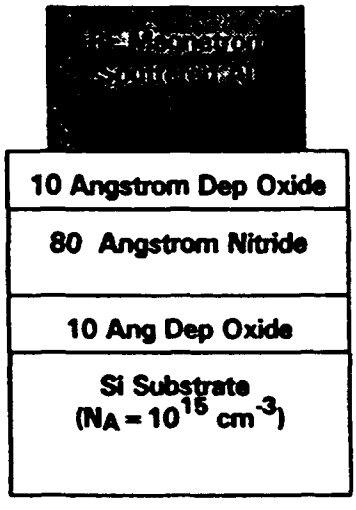


Figure 7 **RPECVD ONO Stack - High Powers and Rates**

- Formation conditions
  - Plasma Power: 30(oxide), 30(nitride) watts
  - Temperature: 300°C
  - Pump/purge cycle time: 15 min with 200 sccm Ar and 100 sccm N_2 at about 0.1 torr
  - Interfacial plasma oxidation time: 3 min
  - Nitride deposition rate: 1.3 Ang/min
- Properties
  - Equivalent oxide thickness: 71 ang
  - Midgap Dit: 6 to $7x10^{11} cm^{-2} eV^{-1}$
  - Hysteresis: 200 mV
  - Ave Breakdown field: 12.5 MV/cm
  - Flatband Voltage : -0.75 V

Charge to Breakdown Summary

- Test Capacitor Area $5x10^{-5}$ cm^2
- Current Density: $1.6x10^{-2}$ A/cm^2
- Oxide Eq Stress Field: 11 MV/cm
- Polarity: Negative gate bias
- Total Charge : 2.8 C/cm^2

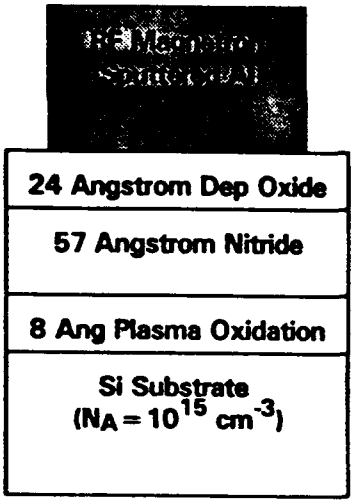
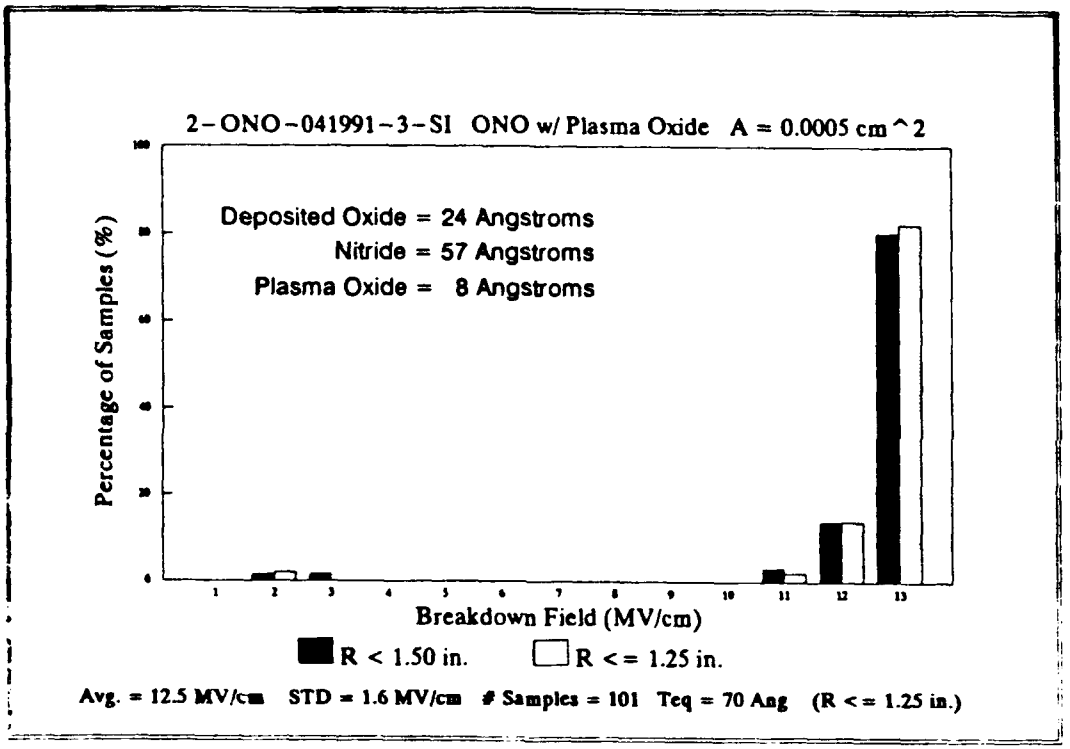


Figure 8 **RPECVD ONO Stack - Plasma Oxidized Interface**



Breakdown Field Histogram

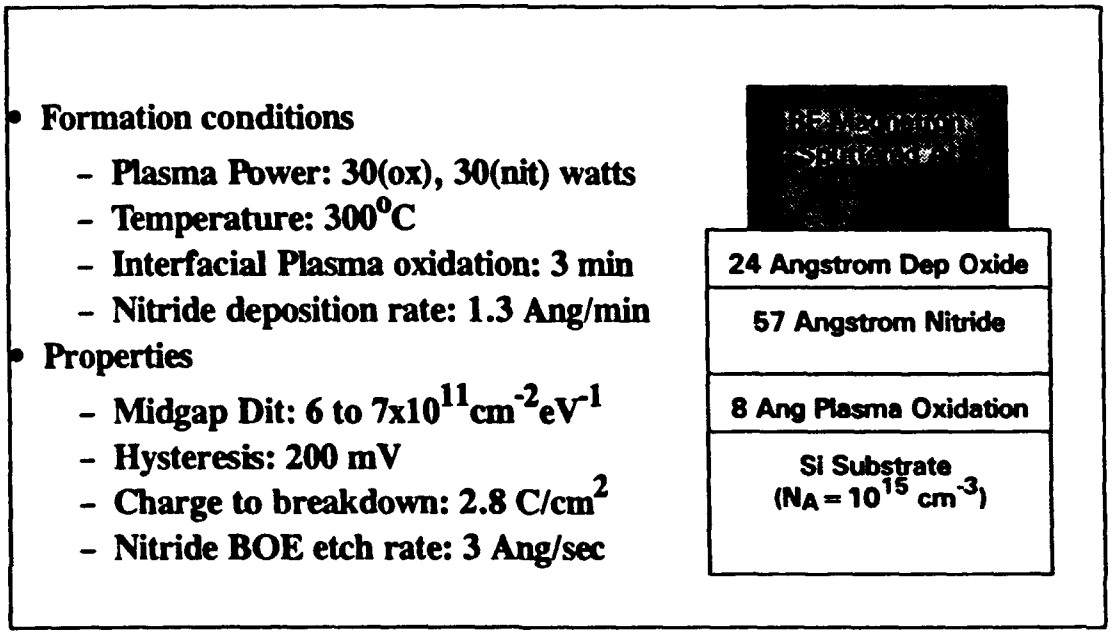
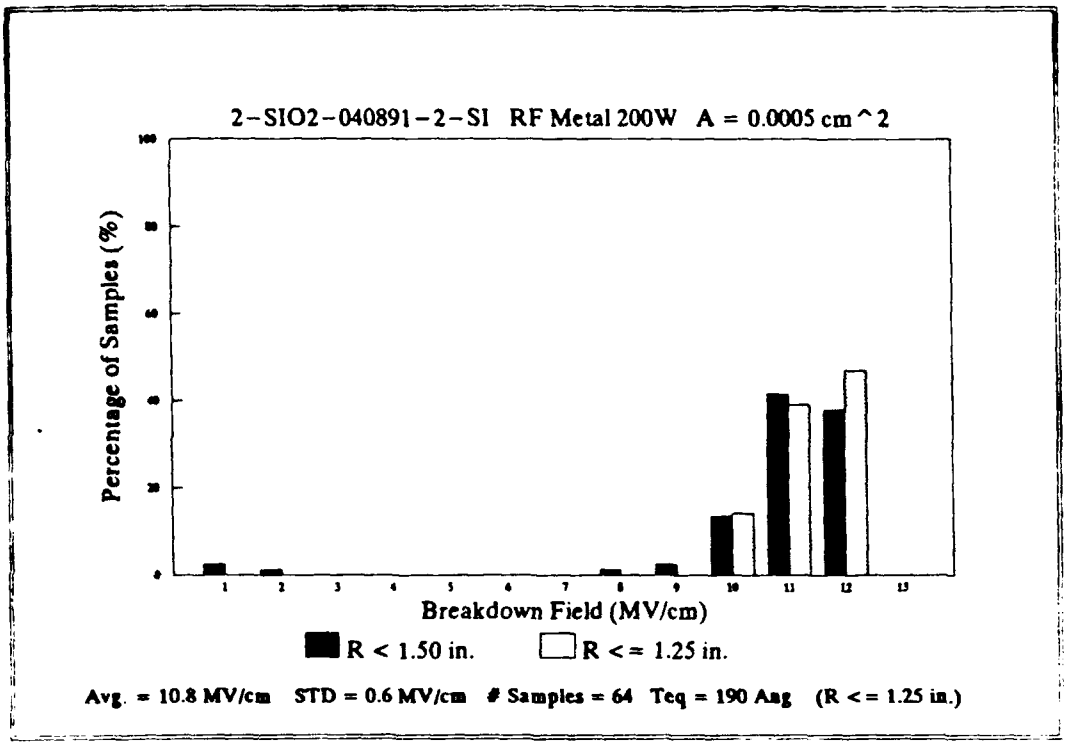


Figure 9 **RPECVD ONO Stack**



Breakdown Field Histogram

- **Deposition conditions**
  - **Plasma Power: 30 watts**
  - **Temperature: 300°C**
  - **Deposition rate: 8 Ang/min**
- **Properties**
  - **Midgap Dit: 2 to $3x10^{10}cm^{-2}eV^{-1}$**
  - **Hysteresis: None**
  - **Charge to breakdown: 0.01 C/cm^2**
  - **Oxide BOE etch rate: 90 Ang/sec**

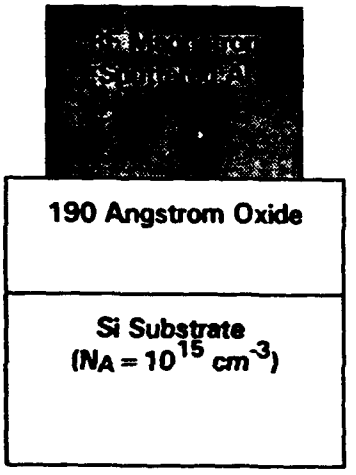
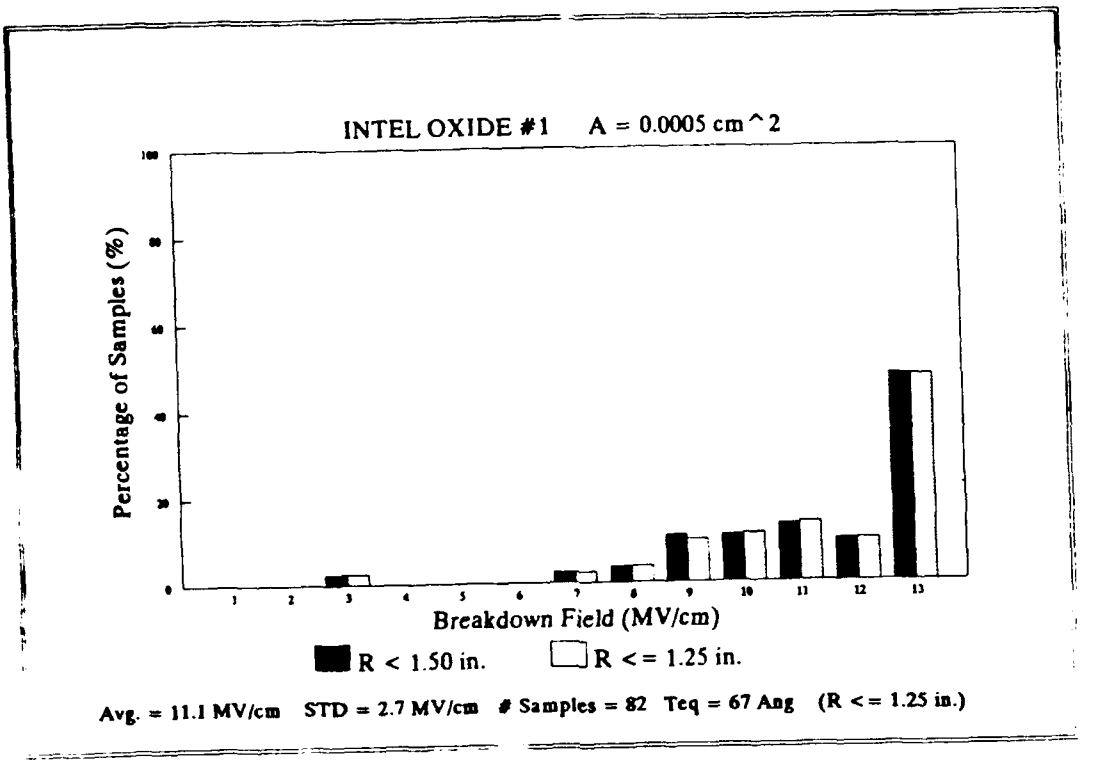


Figure 10 **RPECVD Deposited Oxide**



Breakdown Field Histogram

- **Fabrication conditions**
  - Standard Intel oxide
  - Shipped from west coast
  - Metalized at RTI
- **Properties**
  - Midgap Dit: 2 to $3x10^{10} cm^{-2} eV^{-1}$
  - Hysteresis: None
  - Charge to breakdown: $0.1\ C/cm^2$
  - Oxide BOE etch rate: 12 Ang/sec

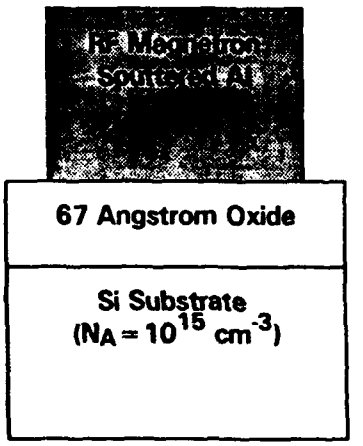


Figure 11 **Thermal Oxide**

7.0 RADIATION TESTING OF DEPOSITED DIELECTRIC STRUCTURES

Radiation testing of oxide, nitride, and ONO samples has continued. ONO samples consistently out perform the oxide and nitride samples.

An interesting trend continues to show up in the deposited oxide samples with thicknesses on the order of 20 nm. The shift in flatband voltage caused by irradiation under bias is proportional to the plasma power used during deposition of the oxide. At 30 watts of plasma deposition power, the flat band shift noted for 1 MRad Si is 1.38 volts. For 200 watts of plasma power the shift is 2.6 volts. For 300 watts of plasma power, the shift is again 2.6. In addition all oxide structures showed significant increases in interface state density. Regardless of the initial value, the final value was typically in the mid 10^{11} to the low 10^{12} cm^{-2} eV^{-1} range. This trend was noted during the last year however little progress has been made towards determining the cause of the decreased hardness. It is none the less interesting to note that an ONO structure formed using a high rate high power oxide process for the interfacial oxide layer and for subsequent nitride and oxide layers, exhibited relatively good radiation resistance. This structure exhibited a flatband shift of only 97 mV of shift and very little increase in interface state density (from 2.1 x 10^{11} to 2.4 x 10^{11} cm^{-2} eV^{-1}). The thickness of this ONO was approximately 8.6 nm.

8.0 FUTURE WORK

During the next year of the program, multilayer RPECVD low temperature dielectric structures will be optimized and evaluated with regard to their radiation tolerance. There are 2 principal tasks which must be carried out. First is the formation of the proper interfacial layer of the MOS structure. This layer will be an oxynitride layer formed by an appropriate combination of oxidation, deposition, and nitrification. The second task is to then integrate this layer into a stacked dielectric structure which provides adequate insulation properties and interfacial properties while maintaining its radiation hardness. This task involves optimizing oxide and nitride deposition parameters. The principal parameter of adjustment is the level of RF power driving the plasma. In addition, the performance of rapid thermal oxides (nitrified and as grown) used in conjunction with the RPECVD nitrides will be evaluated. Test structures will consist of sub 10 nm dielectric films with aluminum capacitors fabricated on the films. Evaluation structures will be based on pre and post radiation flatband shift, interface state density, and breakdown voltage. Statistical evaluation of the breakdown voltage will be carried out.